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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/539,678	06/16/2005	Hee-Seop Kim	8054-125 (LW8088PC/US)	8599

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EXAMINER	
ARMAND, MARC ANTHONY	
ART UNIT	PAPER NUMBER
2814	
MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/539,678	KIM ET AL.	
	Examiner	Art Unit	
	MARC ARMAND	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's election without traverse of claims 4-10 in the reply filed on 05/06/2009 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 4,5,8,9 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Yamazaki et al; (Yamazaki) USPAT6, 417,896.

Regarding claim 4, Yamazaki shows in fig.1A-13; an array substrate (301,401) comprising: a first gate line (902); a second gate line (904) that is electrically insulated from the first gate line (902)(fig.10)(col.9,line 45-68); a data line (901) crossing the first and second gate lines (902,904) to define a pixel region (905) that includes first and second regions (fig.10); a first switching device (claim 1) that is electrically connected to the first gate line and the data line; a second switching device (claim 1) that is electrically connected to the second gate line (fig.10); a transmissive electrode that is electrically connected to the second switching device, the transmissive electrode (212,905) being formed in the first region; a reflective electrode (213,905) that is electrically insulated from the transmissive electrode (206), the reflective electrode (213,905) being formed in the second region that is adjacent to the first region; and a

compensating wiring (207,215) that is electrically connected to the first switching device (col.2,line 40-66), the compensating wiring (207,215) facing the reflective electrode (fig.6) and the transmissive electrode with an insulation layer interposed between the compensating wiring and the reflective electrode and between the compensating wiring and the transmissive electrode (fig.6).

Regarding claim 5, Yamazaki shows in fig.1A-13, an array substrate, wherein the first switching device (fig.3-4) corresponds to a first thin film transistor including a gate electrode that is electrically connected to the second gate line, a source electrode that is electrically connected to the data line, and a drain electrode that is electrically connected to the compensating wiring (col.2, line 45-66) (fig.1-13).

Regarding to claim 8, Yamazaki shows in fig.1A-13 an array substrate wherein the second switching device corresponds to the second thin film transistor (125) including a gate electrode that is electrically connected to the first gate line, a source electrode that is electrically connected to the data line, and a drain electrode (124-126) (fig.2-13) that is electrically connected to the transmissive electrode and the compensating wiring (fig.10) (col.2, line 45-66) (fig.1-13).

Regarding claim 9, Yamazaki shows in fig.1A-13 an array substrate further comprising a circuit (fig.2-13) for allowing the first gate line to maintain a first driving signal until the second gate line receives a second driving signal.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 4-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jun et al., (Jun) USPAT 6,040,882 in view of Yamazaki et al; (Yamazaki) USPAT6, 417,896.

Regarding to claim 4, Jun shows in fig.2, an LCD device having : a first gate line (20a,20b)(col.4,line 53) ; a second gate line (20c,20d) that is electrically insulated from the first gate line (20a,20b); a data line (50)(col.4,line 50) crossing the first and second gate lines (20a,20b) to define a pixel region (90) that includes first and second regions (see fig.2); a first switching device (110a) that is electrically connected to the first gate line (20a,20b) and the data line (20b); a second switching device (110b) that is electrically connected to the second gate line (20c,20d); a transmissive electrode (40b) that is electrically connected to the second switching device (110b) , the transmissive electrode (40b) being formed in the first region; a reflective electrode (40a)(col.4,line 40-44) that is electrically insulated from the transmissive electrode (40b), the reflective electrode (40a) being formed in the second region that is adjacent to the first region, the compensating wiring facing the reflective electrode (40a) and the transmissive electrode (40b) with an insulation layer (110) interposed between the compensating wiring (100) and the reflective electrode (40a) and between the compensating wiring (100) and the transmissive electrode (40b).

Jun differs from the claimed invention because he does not explicitly disclose a semiconductor device having a compensating wiring that is electrically connected to the first switching device.

Yamazaki shows in fig.1A-13, a compensating wiring (207,215) that is electrically connected to the first switching device (col.2, line 40-66),

Yamazaki is evidence that ordinary workers skilled in the art would find reasons, suggestions or motivations to modify the device of Jun because it will provide a device

where the off current can be reduced (col.2, line 15-22). Therefore, at the time the invention was made; it would have been obvious to have a semiconductor device having a compensating wiring that is electrically connected to the first switching device because it will provide a device where the off current can be reduced (col.2, line 15-22).

Regarding claim 5, Jun in view of Yamazaki show in fig.2, an LCD device, wherein the first switching device corresponds to a first thin film transistor (110a and 110b) including a gate electrode (20) that is electrically connected to the second gate line (20c, 20d), a source electrode (70) that is electrically connected to the data line (50), and a drain electrode (60) that is electrically connected to the compensating wiring (100).

Regarding claim 6, Jun in view of Yamazaki show in fig.2, an LCD device, wherein the second switching device (110b) corresponds to a second thin film transistor including a gate electrode (20) that is electrically connected to the first gate line (20a, 20b), a source electrode (70) that is electrically connected to a ground voltage, and a drain electrode (60) that is electrically connected to the transmissive electrode (40b).

Regarding claim 7, Jun in view of Yamazaki show in fig.2, an LCD device having a third thin film transistor (110c) that includes a gate electrode that is electrically connected to the first gate line (20), a source electrode (70) that is electrically connected to the data line (20), and a drain electrode (60) that is electrically connected to the compensating wiring (40a).

Regarding claim 8, Jun in view of Yamazaki show in fig.2, an LCD device having a second switching device (110b) corresponds to the second thin film transistor including a gate electrode that is electrically connected to the first gate line (20a, 20b), a source electrode (70) that is electrically connected to the data line (20), and a drain electrode that is electrically connected to the transmissive electrode (40b) and the compensating wiring (40a).

Regarding claim 9, Jun in view of Yamazaki show in fig.2, an LCD device having a circuit for allowing the first gate line (20a,20b) to maintain a first driving signal until the second gate line (20c,20d) receives a second driving signal.

Regarding to claim 10, Jun in view of Yamazaki show in fig.2, an LCD device wherein the compensating wiring (100) and the data line (50) are formed from a same layer (co.4,line 63).

Response to Arguments

7. Applicant's arguments with respect to claims 4-10 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MARC ARMAND whose telephone number is (571)272-9751. The examiner can normally be reached on 9-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MARC ARMAND/
Examiner, Art Unit 2814

/Wael M Fahmy/
Supervisory Patent Examiner, Art Unit 2814